☆☆☆ <u>Updating of FBs OS V4.23</u>   6/8/2005

● Supporting the working interface for FBs-2A1D/FBs-2DA on-board analog modules, the related interface registers are as below :

. D4071 : This register shows the installation information

High Byte = 5AH, main unit with intelligent board
= Other values, main unit without intelligent board

Low Byte = 1, on-board is FBs-CBE
= 2, on-board is FBs-B2A1D
= 3, on-board is FBs-B2DA

Value of D4071	Port 1 Comm. Interface	Analog Interface
5A01H (Main unit with FBs-CBE)	.FATEK protocol only .Comm. parameters .Baud Rate : 115200 bps .Data Bit : 7-bit .Parity : Even .Stop Bit : 1-bit .M1960=0, Port 1 is busy .R4040 High Byte=0, Non delay for reply	None

5A02H (Main unit with FBs-B2A1D)	. FATEK protocol only
	
	. Comm. parameters
	 .Baud Rate : 104727 bps
	 .Data Bit : 7-bit
	 .Parity : Even
	 .Stop Bit : 1-bit
	.M1960=0, Port 1 is busy
	.R4040 High Byte=0,
	 Non delay for reply
		.Analog Input : 2 channels
		.Analog Output : 1 channel
		.Resolution : 12-bit
		.Data Format : 14-bit, but valid12-bit
		.Type of Signal :
		 Voltage: 0～10V / Current: 0～20mA
		.Without isolation between channels
		.D4072 : 1_{ST} Analog Input Register
		    (0～16380)
		.D4073 : 2_{nd} Analog Input Register
		    (0～16380)
		.D4076 : 1_{ST} Analog Output Register
		    (0～16380)

5A03H (Main unit with FBs-B2DA)	. FATEK protocol only
	
	. Comm. parameters
	 .Baud Rate : 104727 bps
	 .Data Bit : 7-bit
	 .Parity : Even
	 .Stop Bit : 1-bit
	.M1960=0, Port 1 is busy
	.R4040 High Byte=0,
	 Non delay for reply
		.Analog Output : 2 channels
		.Resolution : 12-bit t
		.Data Format : 14-bit, but valid12-bit
		. Type of Signal :
		 Voltage: 0～10V / Current: 0～20mA
		. Without isolation between channels
		.D4076 : 1_{ST} Analog Output Register
		    (0～16380)
		.D4077 : 2_{nd} Analog Output Register
		    (0～16380)

.Data format of 14-bit, but valid 12-bit representation (0～16380) :

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0

● Floating point instructions (FUN200~FUN213) may combine with V、Z、P0~P9 to serve indirect addressing application.

● Adding the malfunction detection for main unit power failure detection circuit and force entering STOP operation mode while the execution of illegal system reset. If under such situation, the ERR indicator flickers in 1 Hz frequency, and the corresponding indications are as below:
. The output indicators Y3=ON, Y2=OFF, Y1=ON, Y0=ON
. The register R4049 will contain the value 11

● Modify the internal display mode for Input/Output、RUN、ERR indicators while PLC main unit stays at STOP or ERROR mode.

● When upgrading the PLC OS firmware version V4.20 or later, it needs version V1.03 of the update utility Os_update.exe for working.