The major H/W specifications of FB-series PLC

Items	Special I/O	MA		MC		FBN
Model of main unit		FB-xxMA	FBE-xxMA	FB-xxMC	FBE-xxMC	FBN-xxMC
OS version		V2.xx	V3.xx	V2.xx	V3.xx	V3.xx
Clock of CPU		10MHz	20MHz	10MHz	20MHz	20MHz
Basic execution time		0.66uS	0.33uS	0.66uS	0.33uS	0 .33uS
Program memory		8KW	8/13KW	8KW	8/13KW	8/13KW
I/O terminal block		Detachable	Detachable	Detachable	Detachable	Detachable
Input interface		Sink	Sink/Source	Sink	Sink/Source	Sink/Source
Inverse of input (main unit)		-----	-----	-----	Yes	Yes
Output interface (Transistor)		Sink	Sink/Source	Sink	Sink/Source	Sink/Source
Inverse of output (main unit)		-----	-----	-----	Yes	Yes
Communication port 0		9600 7-bit,Even,1	9600～38400 7-bit,Even,1	9600 7-bit,Even,1	9600～38400 7-bit,Even,1	9600～38400 7-bit,Even,1
Communication port 1 (FUN97 allowed)		-----	-----	600～19200 Adjustable	600～38400 Adjustable	600～38400 Adjustable
Communication port 2 (FUN96 allowed)		-----	-----	-----	4800～614.4K Adjustable	4800～614.4K Adjustable
High speed inputs	X0~X7	4K Hz .SHSC: HSC2,3 Total 8KHz *1	4KHz .SHSC: HSC2,3 Total 8KHz *1	10KHz (U/D) 5KHz (A/B) .HHSC: HSC0,1 .Interrupt input .SHSC HSC2～7 Total 8KHz *2	20KHz (U/D) 10KHz (A/B) .HHSC: HSC0,1 .Interrupt input .SHSCH: HSC4～7 Total 8KHz *3	512KHz (Diff) or 20/10 KHz .HHSC: HSC0,1 .Interrupt input .SHSC: HSC4～7 Total 8KHz *4
High speed inputs	X8~X15	-----	-----	-----	20KHz (U/D) 10KHz (A/B) .HHSC: HSC2,3 .Interrupt input .SHSC: HSC4～7 Total 8KHz *3	512KHz (Diff) or 20/10 KHz .HHSC: HSC2,3 . Interrupt input .SHHC: HSC4～7 Total 8KHz *4
Modes of high speed input		 .SHSC: U/D	 .SHSC: U/D,K/R, A/B	.HHSC: U/D,A/B .Interrupt input: Positive edge .SHSC: U/D	.HHSC: U/D,U/D×2 K/R,K/R×2 A/B,A/B×2 A/B×3,A/B×4 .Interrupt input: Positive edge, Negative edge or Both .SHSC: U/D,K/R,A/B	.HHSC: U/D,U/D×2 K/R,K/R×2 A/B,A/B×2 A/B×3,A/B×4 .Interrupt input: Positive edge, Negative edge or Both .SHSC: U/D,K/R,A/B
Pulse output via FUN81	Y0～Y15	-----	8～2KHz .Mode: U/D,K/R	8～2KHz .Mode: U/D,K/R	8～2KHz .Mode: U/D,K/R	8～2KHz .Mode: U/D,K/R

Pulse output via FUN140	Y0～Y7	-----	-----	-----	10～20KHz (U/D,K/R) 10～10KHz (A/B) .HSPSO: PS0～3 .Mode: U/D,K/R,A/B *5	10～512KHz (Diff) 10～20/10 KHz (U/D,K/R,A/B) .HSPSO: PS0～3 .Mode: U/D,K/R,A/B *6
0.1mS H/W high speed timer		-----	-----	-----	.HSTA .HST0,HST1 HST2,HST3 *7	.HSTA .HST0,HST1 HST2,HST3 *7
Fixed time interrupt		-----	1MSI,2MSI 3MSI,4MSI 5MSI,10MSI 50MSI, 100MSI	10MS,20MS 30MS,40MS 50MS,60MS 70MS,80MS 90MS,100MS	1MSI,2MSI 3MSI,4MSI 5MSI,10MSI 50MSI,100MSI	1MSI,2MSI 3MSI,4MSI 5MSI,10MSI 50MSI,100MSI

*1: The MA main unit may support 2 sets of software high speed counter (SHSC) HSC2～HSC3 via the configuration of X0～X7

*2: The FB-xxMC (V2.xx) main unit may support 2 sets of hardware high speed counter (HHSC) HSC0～HSC1 and/or upto 6 sets of software high speed counter HSC2～HSC7 via the configuration of X0～X7

*3: FBE-20MC(V3.xx) main unit may support 3 sets of hardware high speed counter HSC0～HSC2 and/or upto 4 sets of software high speed counter HSC4～HSC7 via the configuration of X0～X11

FBE-28/40MC(V3.xx) main unit may support 4 sets of hardware high speed counter HSC0～HSC3 and/or upto 4 sets of software high speed counter HSC4～HSC7 via the configuration of X0～X15

※ For the compatability with FB-xxMC (V2.xx), FBE-xxMC(V3.xx) may support HSC2 and HSC3 as the software high speed counter via the configuration of X0～X7

※ Total frequency of interrupt inputs and inputs of software high speed counter can't exceed 8K Hz

*4: FBN-19MC(V3.xx) main unit may support 1 set of hardware high speed counter HSC0 (upto 512 K Hz) via the configuration of X0～X3 (differential inputs, without X2) , 2 sets of hardware high speed counter HSC1～HSC2 , and/or upto 4 sets of software high speed counter HSC4～HSC7 via the configuration of X4～X11(Single-ended inputs)

FBN-26MC(V3.xx) main unit may support 2 sets of hardware high speed counter HSC0～HSC1 (upto 512 K Hz) via the configuration of X0～X7 (differential inputs, without X2 & X6) , 2 sets of hardware high speed counter HSC2～HSC3 , and/or upto 4 sets of software high speed counter HSC4～HSC7 via the configuration of X8～X15 (Single-ended inputs)

FBN-36MC(V3.xx) main unit may support 4 sets of hardware high speed counter HSC0～HSC3 (upto 512 K Hz) via the configuration of X0～X15 (differential inputs, without X2&X6&X10&X14) , and/or upto 4 sets of software high speed counter HSC4～HSC7

※ Total frequency of interrupt inputs and inputs of software high speed counter can't exceed 8K Hz

*5: FBE-20MC(V3.xx) main unit may support 1 set of high speed pulse output (HSPSO) PSO0 via the configuration of Y0～Y1

FBE-28MC(V3.xx) main unit may support 2 sets of high speed pulse output PSO0～PSO1 via the configuration of Y0～Y3

FBE-40MC(V3.xx) main unit may support 4 sets of high speed pulse output PSO0～PSO3 via the configuration of Y0～Y7

*6: FBN-19MC(V3.xx) main unit may support 1 set of high speed pulse output PSO0 (upto 512K Hz) via the configuration of Y0～Y1 (Differential output)

FBN-26MC(V3.xx) main unit may support 2 set of high speed pulse output PSO0～PSO1 (upto 512K Hz) via the configuration of Y0～Y3 (Differential output)

FBN-36MC(V3.xx) main unit may support 4 set of high speed pulse output PSO0～PSO3 (upto 512K Hz) via the configuration of Y0～Y7 (Differential output)

*7: FBE-xxMC(V3.xx) and FBN-xxMC(V3.xx) main unit has built in 1set of 0.1mS hardware high speed timer (HSTA) and 4 sets of hardware high speed counter (HSC0～HSC3) or 4 sets of 0.1mS hardware high speed timer (HST0～HST3)

The range of the operands

Type	V2.xx	V3.xx	Comment
Discrete Input	X0～X159	X0～X255	
Discrete Output	Y0～Y159	Y0～Y255	
Timer	T0～T255	T0～T255	
Counter	C0～C255	C0～C255	
Internal M Relay	M0～M1399	M0～M1911	
Step Relay	S0～S999	S0～S999	
Special M Relay	M1912～M2001	M1912～M2001	
Data Register Rxxxx	R0～R3839	R0～R3839	
Analog Input Register	R3840～R3847	R3840～R3903	
Analog Output Register	R3904～R3911	R3904～R3967	
Special Register	R3968～R4167	R3968～R4167	
Read Only Register	R5000～R8071	R5000～R8071	Set the Read Only Registers (ROR) via the configuration
Data Register Rxxxx	---	R5000～R8071	R5000～R8071 will act like the general purpose registers if they are not defined as ROR
Data Register Dxxxx	---	D0～D3071	
Index Register	---	V,Z	For indirect addressing