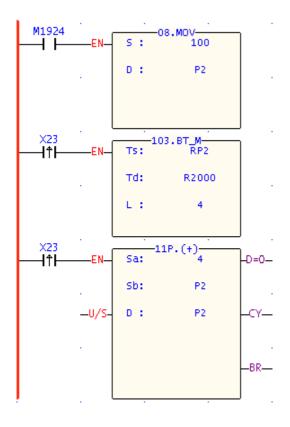
Description for V ⋅ Z & P0 ~ P9 Index Register

- The FBS series PLC (OS version V4.XX) supports $V \cdot Z \& P0 \sim P9$ in total 12 index registers for indirect addressing application.
- In indirect addressing application, Rxxxx register can combine $V \cdot Z \& P0 \sim P9$ for index addressing; Dxxxx register can't combine $V \cdot Z$ for index addressing, but $P0 \sim P9$ are allowed.
- When V · Z index register being combined with the Rxxxx register, for example, R0 with V · Z, the instruction format is R0V(where V=100, it means R100) or R0Z(where Z=500, it means R500); when P0 ~ P9 index register being combined with the Rxxxx register, the instruction format is RPn (n=0~9) or RPmPn (m,n=0~9), for example RP5 (where P5=100, it means R100) or RP0P1(where P0= 100, P1=50, it means 150).
- When P0 \sim P9 index register being combined with the Dxxxx register, the instruction format is DPn (n=0 \sim 9) or DPmPn (m,n=0 \sim 9), for example DP3 (where P3=10, it means D10) or DP4P5 (where P4=100, P5=1, it means D101).
- It can combine both P0~P9 index register, for example P2=20, P3=30, when Rxxxx or Dxxxx register combines both index register, RP2P3 will point to R50, DP2P3 will point to D50, it means the summation of both index register for indirect addressing.



- Index register P2=100 while power up or first run.
- When X23 changes from 0→1, FUN103 will perform the table movement, the source starts from R100 (P2=100), the destination starts from R2000, the amount is 4. Coping the content of R100~R103 for R2000~R2003 at first execution, coping the content of R104~R107 for R2000~R2003 at second execution...
- Increasing the P2 index register by
 4 to point to next 4 words.