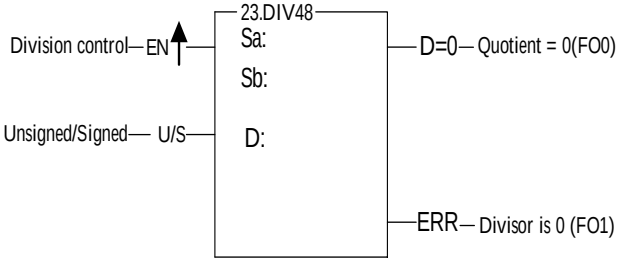
FUN 23 DIV48	48-BIT DIVISION	FUN 23 DIV48

Ladder Symbol



Sa：Starting register of dividend
Sb：Starting register of divisor
D ：Starting register to store the result (quotient)
Sa, Sb may combine with V、Z、P0~P9 to serve indirect addressing

Range / Operand	HR	OR	SR	ROR	DR	XR
	R0 | R3839	R3904 | R3967	R3968 | R4167	R5000 | R8071	D0 | D4095	V、Z P0~P9
Sa	○	○	○	○	○	○
Sb	○	○	○	○	○	○
D	○	○	○*	○*	○	○

- When operation control “EN”=1 or “EN ↑ ” (P instruction) changes from 0→1, it will perform the signed (unsigned/signed input "U/S"=0) or unsigned (unsigned/signed input "U/S"=1) 48-bit division operation. Dividend and divisor are each formed by three consecutive registers starting by Sa and Sb respectively. If the result is zero, ‘D=0’ output will be set to 1. If divisor is zero then the ‘ERR’ will be set to 1 and the resultant register will keep unchanged.
- All operands involved in this function are all 48-bit, so Sa, Sb and D are all comprised by 3 consecutive registers.

Example: Signed 48-bit division

In this example dividend formed by register R2, R1, R0 will be divided by divisor formed by register R5, R4, R3. The quotient will store in R8, R7, and R6.

	Sa	R2	R1	R0
		2147483647		
÷	Sb	R5	R4	R3
		1234567		
		R8	R7	R6
		1739		
		Quotient		