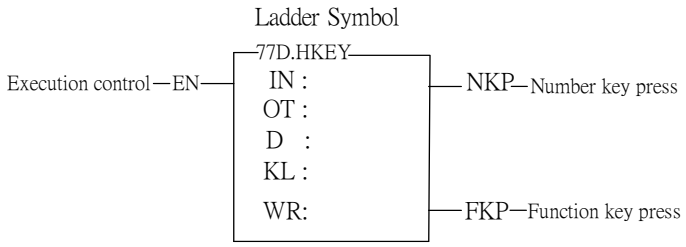
FUN 77 HKEY	HEX-KEY INPUT	FUN 77 HKEY

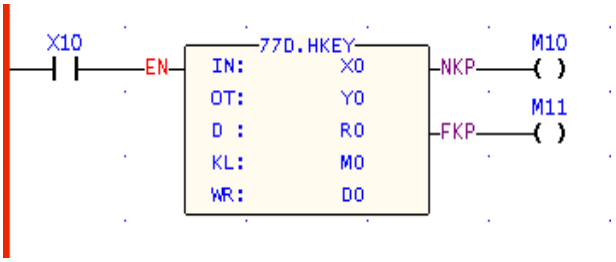
Ladder Symbol



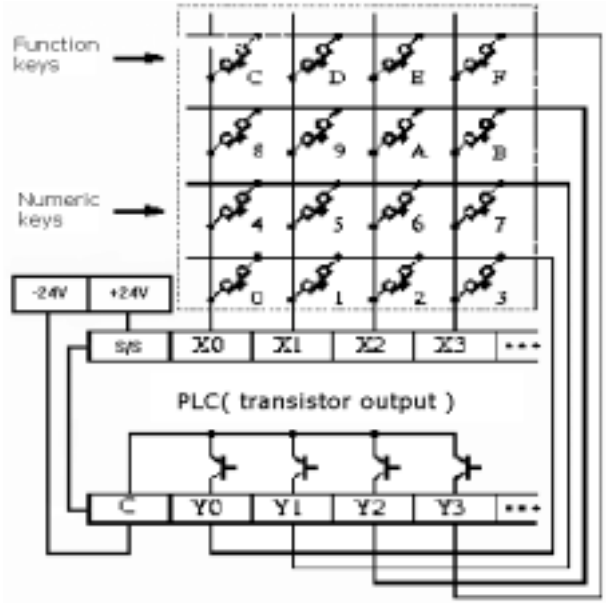
IN : Starting of digital input for key scan
OT: Starting of digital output for multiplexing key scan (4 points)
D : Register to store key-in numbers
KL : Starting relay for key status
WR: Working register, it can't repeat in use
D may combine with V、Z、P0~P9 to serve indirect addressing application

Range / Ope-rand	X	Y	M	S	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	XR
	X0 | X240	Y0 | Y240	M0 | M1896	S0 | S984	WY0 | WY240	WM0 | WM1896	WS0 | WS984	T0 | T255	C0 | C255	R0 | R3839	R3904 | R3967	R3968 | R4167	R5000 | R8071	D0 | D4095	V、Z P0~P9
IN	○														
OT		○													
D					○	○	○	○	○	○	○	○*	○*	○	○
KL		○	○	○											
WR										○			○*	○	

- The numeric (0~9) key function of this instruction is similar as for the TKEY instruction. The hardware connection for TKEY and HKEY is different. For TKEY instruction each key have one input point to connect, while HKEY use 4 input points and 4 output points to form a 4x4 multiplex 16 key input. 4×4 means that there can be 16 input keys, so in addition to the 10 numeric keys, the other 6 keys can be used as function keys (just like the usual discrete input). The actions of the numeric keys and the function keys are independent and have no effect on each other.
- When execution control "EN" = 1, this instruction will scan the numeric keys and function keys in the matrix formed by the 4 input points starting from IN and the 4 output points starting from OT. For the function of the numeric keys and "NKP" output please refer to the TKEY instruction. The function keys maintain the key-in status of the A~F keys in the last 6 relays specified by KL (the first 10 store the key-in status of the numeric keys). If any one of the A~F keys is depressed, FKP (FO1) will set to 1. The OT output points for this instruction must be transistor outputs.
- The biggest number for a 16-bit operand is 4 digits (9999), and for 32-bit operand is 8 digits (99999999). However, there are only 6 function keys (A~F), no matter whether it is a 16-bit or 32-bit operand.

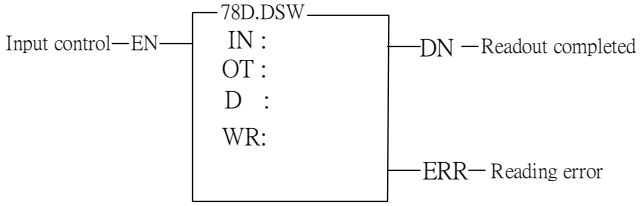


• The instruction in the diagram above uses X0~X3 and Y0~Y3 to form a multiplex key input. It can input numeric values of 8 digits and stores the results in R1R0. The input status of the function keys is stored in M10(A)~M15(F).



FUN 78 DSW	DIGITAL SWITCH INPUT	FUN 78 DSW

Ladder Symbol

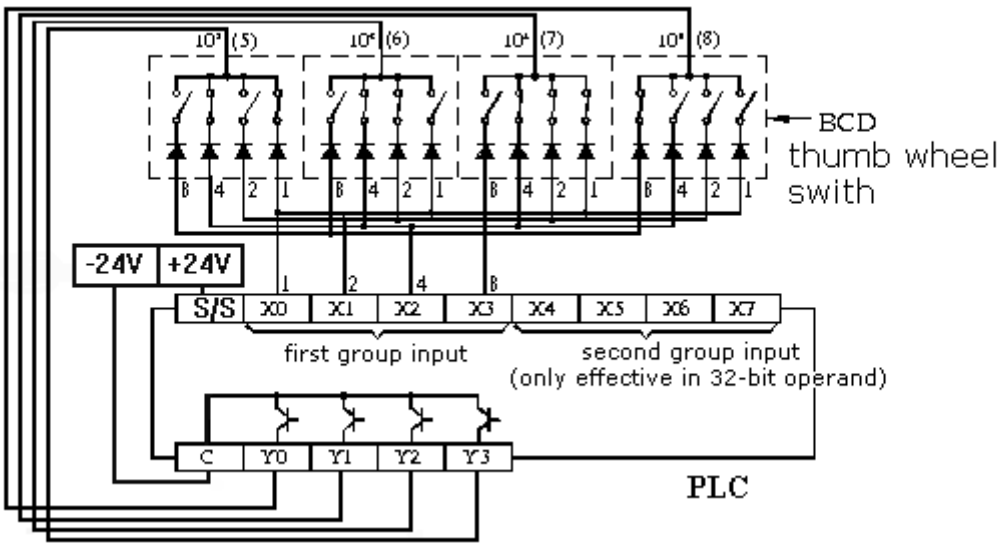


IN : Starting of input for thumb wheel switch
OT: Starting of output for multiplexing scan (4 points)
D : Register to store readout value
WR: Working register, it can't repeat in use (WR & WR+1 for 16-bit operation; WR, WR+1 & WR+2 for 32-bit operation)
D may combine with V、Z、P0~P9 to serve indirect addressing application

Operand \ Range	X	Y	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	XR
	X0 | X240	Y0 | Y240	WY0 | WY240	WM0 | WM1896	WS0 | WS984	T0 | T255	C0 | C255	R0 | R3839	R3904 | R3967	R3968 | R4167	R5000 | R8071	D0 | D4095	V、Z P0~P9
IN	○												
OT		○											
D			○	○	○	○	○	○	○	○*	○*	○	○
WR								○			○*	○	

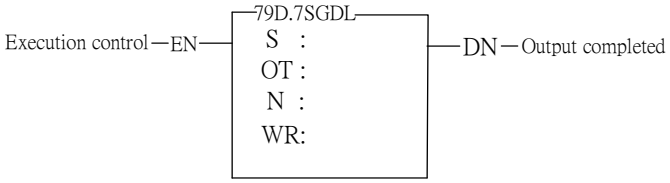
- When input control "EN" = 1, this instruction will readout one digit data from the 4 input points starting from IN (IN0~IN3). It takes 4 scans to read out a group of 4-digit BCD values (0000~9999) and store them into D register. With a 32-bit operand, each scan can get 2 digits of data by reading the additional digit from IN4-IN7 and store it in the D+1 register. Each bit of OT0~OT3 will sequentially set to 1 and get the digit data respectively into 10^0(ones), 10^1(tens), 10^2(hundreds), and 10^3(thousands). As long as EN is 1, PLC will scan and read out in continuous cycles. When each complete cycle is finished (i.e. the 4 digit readout of 10^0~10^3 is completed), the readout completed flag "DN" is set to 1. However, it is only kept for one scan. If any digital readout value is not within the range of 0~9 (BCD), then reading error "ERR" will be set to 1 and the value of that group of digits will be set to 0000.
- The output points must be transistor outputs.

- In this example, when X10 is 1, then the numeric value of the thumb wheel switch (5678 in this example) will be read out and stored into the R0 register.
- The bits (8,4,2,1) with same digit should be connect together and series with a diode (as shown in diagram below).
- With 32-bit operand a set of similar thumb wheel switch may be added to X4~X7 (Y0~Y3 are shared with another group).



FUN 79 7SGDL	7-SEGMENT OUTPUT WITH LATCH	FUN 79 7SGDL

Ladder Symbol



S : Register storing the data (BCD) to be displayed

OT : Starting number of scanning output

N : Specify signal output and polarity of latch

WR : Working register, it can't repeat in use

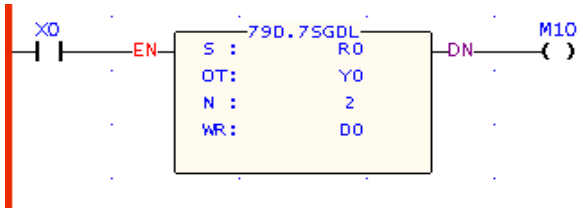
S may combine with V、Z、P0~P9 to serve indirect addressing application

Range / Operand	Y	WX	WY	WM	WS	TMR	CTR	HR	IR	OR	SR	ROR	DR	K	XR
	Y0 | Y240	WX0 | WX240	WY0 | WY240	WM0 | WM1896	WS0 | WS984	T0 | T255	C0 | C255	R0 | R3839	R3840 | R3903	R3904 | R3967	R3968 | R4167	R5000 | R8071	D0 | D4095	16-bit number	V、Z P0~P9
S			○	○	○	○	○	○	○	○	○	○	○	○	○
OT	○														
N														0～3	
WR								○				○*	○		

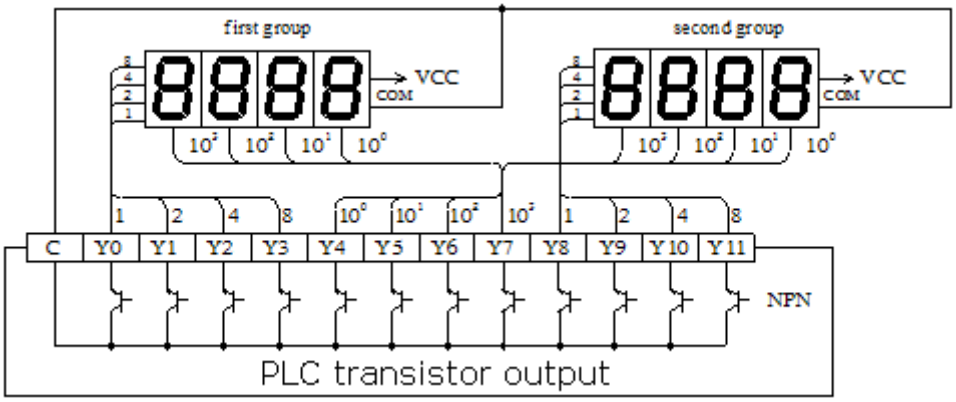
- When input control "EN" = 1, the 4 nibbles of the S register, from digit 0 to digit 3, are sequentially sent out to the 4 output points, OT0~OT3. While output the digit data, the latch signal of that digit (OT4 corresponds to digit 0, OT5 corresponds to digit 1, etc...) at the same time is also sent out so that the digital value will be loaded and latched into the 7-segment display respectively.

- When in D (32-bit) instruction, nibbles 0~3 from the S register, and nibbles 0~3 from the S+1 register are transferred separately to OT0~OT3 and OT8~OT11. Because they are transferred at the same time, they can use the same latch signal. 16-bit instructions do not use OT8~OT11.

- As long as "EN" remains 1, PLC will execute the transfer cyclically. After each transfer of a complete group of numerical values (nibbles 0~3 or 0~7), the output completed flag "DN" will set to 1. However, it will only be kept for 1 scan.



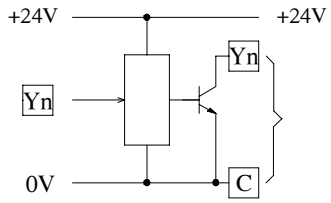
- In this example, when X0=1, the 4 nibbles of R0 will be transferred to the first group 7-segment display in the diagram below. The 4 nibbles of R1 will be transferred to the second group 7-segment display.



FUN 79 7SGDL	7-SEGMENT OUTPUT WITH LATCH	FUN 79 7SGDL

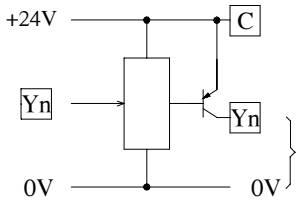
- FATEK PLC's transistor output has both a negative logic transistor output (NPN transistor - when the output status is ON, the terminal voltage of the transistor output is low), and a positive logic transistor output (PNP - when the output status is ON, the terminal voltage of the transistor output is high). Their structure is as follows:

FBs-PLC negative logic output (NPN transistor)



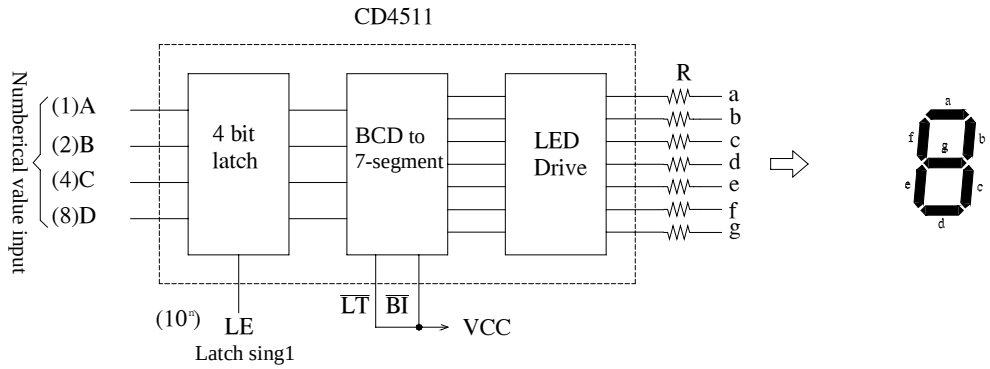
When Yn is "ON", this output voltage is low

FBs-PLC positive logic output (PNP transistor)



When Yn is "ON", Yn's terminal voltage is high

- The data inputs (8,4,2,1) and latch signals of the 7-segment displays on the shelf for positive and negative logic are all available. For example, for numerical value "8", the positive logic input should be 1000, and the negative logic input 0111. Similarly, when the latch signal is 0, the positive logic latch permits the display numerical values to enter through the latch (i.e. be loaded). When the latch signal is 1, the numerical values in the latch are latched (maintained), and with negative logic they are not. The following diagram of a CD-4511 7-segment display IC is an example of a positive logic numerical value input with latch.



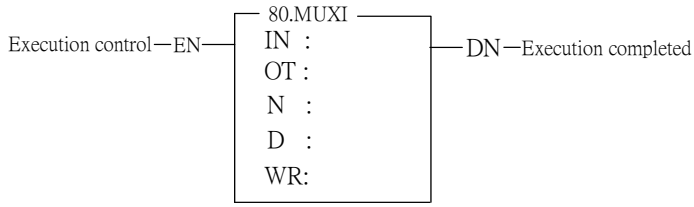
- Because the PLC output and the 7-segment display input polarity can be positive and negative logic. Therefore, the polarities between output and input must be coordinated to get the correct result. This instruction uses N to specify the polarity relation between the PLC transistor output, and the 7-segment display. The table below shows all the possibility.

Numerical value input (8~1)	Latch signal (10^0-10^3)	Value of N
Same	Same	0
	Different	1
Different	Same	2
	Different	3

- In the diagram above, CD4511 is used as an example. If use NPN output, the data input polarity is different to PLC, and its latch input polarity is the same as PLC, so N value should chosen as 2.

FUN 80 MUXI	MULTIPLEX INPUT	FUN 80 MUXI

Ladder Symbol



IN : Starting of multiplexing input

OT: Starting of output for multiplexing scan (must be transistor output)

N : Multiplex input lines (2~8)

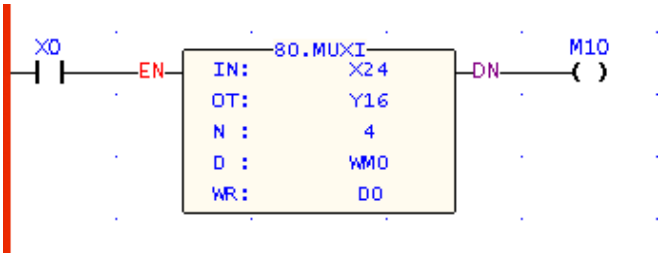
D : Register for storing inputs

WR: Working register, it can't repeat in use

D may combine with V、Z、P0~P9 to serve indirect addressing application

Operand \ Range	X	Y	WY	WM	WS	TMR	CTR	HR	OR	SR	ROR	DR	K	XR
	X0 | X240	Y0 | Y240	WY0 | WY240	WM0 | WM1896	WS0 | WS984	T0 | T255	C0 | C255	R0 | R3839	R3904 | R3967	R3968 | R4167	R5000 | R8071	D0 | D4095	2 | 8	V、Z P0~P9
IN	○													
OT		○												
N													○	
D			○	○	○	○	○	○	○	○*	○*	○		○
WR								○			○*	○		

- This instruction uses the multiplex method to read out N lines of input status from 8 consecutive input points (IN0~IN7) starting from the input point specified by IN. With this method we can obtain 8×N input status, but only need to use 8 input points and N output points.
- The multiplex scanning method goes through N output points starting from the OT output point. Each scan one of the N bits will set to 1 and the corresponding line will be selected. OT0 responsible for first line, while OT1 responsible for second line, etc. Until it read all the N lines the 8×N status that has been read out is then stored into the register starting at D, and the execution completed flag "DN" is set as 1 (but is only kept for one scanning period).
- With every scan, this instruction retrieves a line for 8 input status, so N lines require N scan cycles before they can be completed.



- This example retrieves 4 lines×8 points of input, 32 point status in all. They are stored into the 32-bit register of DWM0 (M0~M31).